LP3936 Lighting Management System for Six White LEDs and One RGB or FLASH LED

Check for Samples: LP3936

FEATURES

- **High Efficiency 250 mA Magnetic Boost DC-DC Converter with Programmable Output Voltage**
- **PWM controlled RGB LED drivers with programmable color, brightness, turn on/off slopes and blinking**
- **FLASH function with 3 drivers, each up to 120 mA current**
- **4 constant current White LED drivers with programmable 8-bit adjustment (0 … 25 mA/LED)**
- **2 constant current White LED drivers with programmable 8-bit adjustment (0 … 25 mA/LED)**
- **8-bit ADC for ambient light sensor with averaging**
- **Combined MicroWire/SPI and I^2C compatible serial interface**
- **Low current Standby mode (software controlled)**
- **Low voltage digital interface down to 1.8V**
- **Space efficient 32-pin TLGA laminate package**

APPLICATIONS

- **Cellular Phones**
- **PDAs**

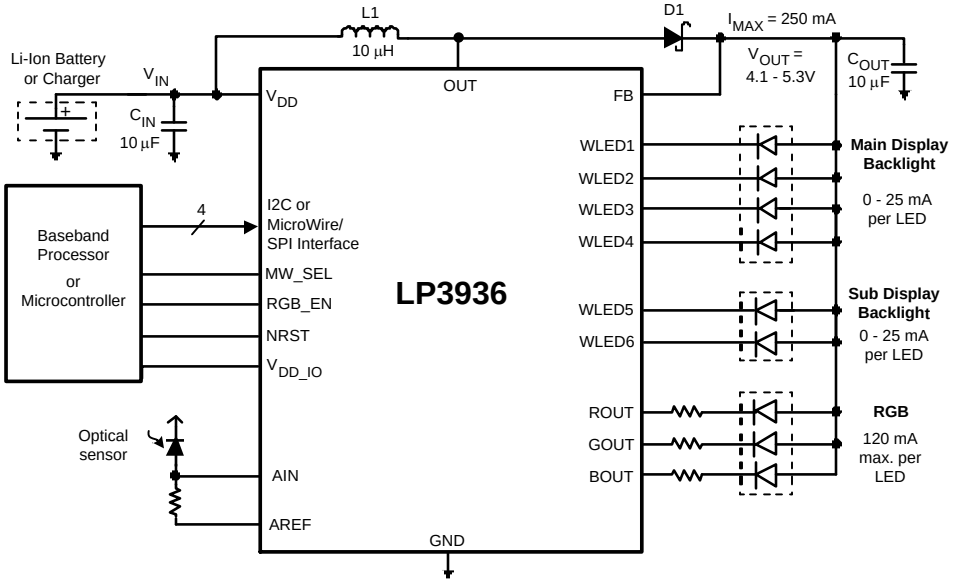
DESCRIPTION

LP3936 is a complete lighting management system designed for portable wireless applications. It contains a boost DC/DC converter, 4 white LED drivers to drive the main LCD panel backlight, 2 white LED drivers for sub-LCD panel and 1 set of RGB LED drivers.

Both WLED groups have 8-bit programmable constant current drivers that are separately adjustable and matched to 1% (typ.). For efficient backlighting the backlight intensity can be adjusted using the 8-bit ADC with ambient light detection circuit.

The RGB LED drivers are PWM-driven with programmable color, intensity and blinking patterns. In addition, they feature a FLASH function to support picture taking with camera-enabled cellular phones.

Typical Application



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DESCRIPTION (CONTINUED)

An efficient magnetic boost converter provides the required bias operating from a single Li-Ion battery. The DC/DC converter output voltage is user programmable for adapting to different LED types and for efficiency optimization. All functions are software controllable through an I^2C and MicroWire/SPI compatible interface and 16 internal registers.

Connection Diagrams and Package Mark Information

32-Lead TLGA Package, 4.5 x 5.5 x 0.8 mm, 0.5 mm pitch

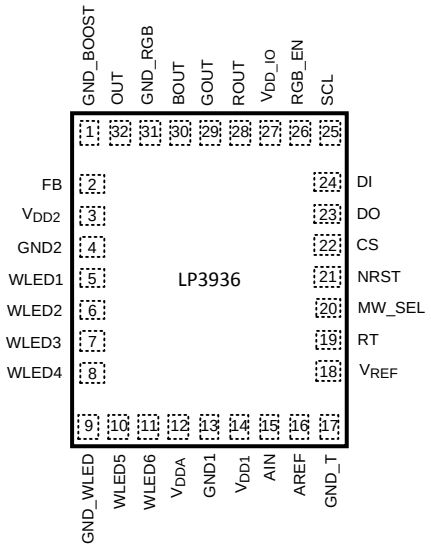

Figure 1. TLGA Package – Top View
See Package Number NPC0032A

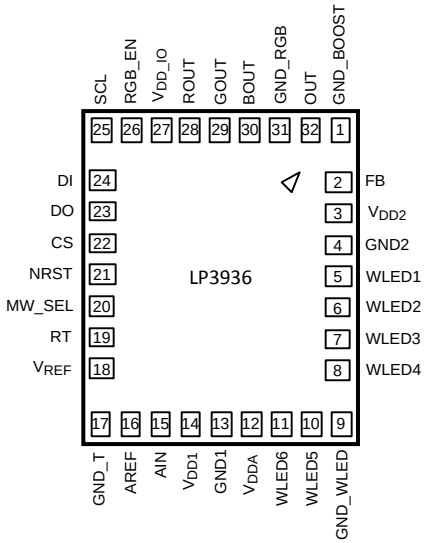

Figure 2. TLGA Package – Bottom View

Pin Description

Pin	Name	Type	Description
1	GND_BOOST	Ground	Power Switch Ground
2	FB	Input	Boost Converter Feedback
3	V_{DD2}	Power	Supply Voltage for Internal Digital Circuits
4	GND2	Ground	Ground Return for V_{DD2} (Internal Digital)
5	WLED1	LED Output	Open Drain, White LED1 Output
6	WLED2	LED Output	Open Drain, White LED2 Output
7	WLED3	LED Output	Open Drain, White LED3 Output
8	WLED4	LED Output	Open Drain, White LED4 Output
9	GND_WLED	Ground	4+2 White LED Driver Ground
10	WLED5	LED Output	Open Drain, White LED5 Output
11	WLED6	LED Output	Open Drain, White LED6 Output
12	V_{DDA}	Output	Internal LDO Output, 2.8V
13	GND1	Ground	Ground Return for V_{DD1} (Internal Analog)
14	V_{DD1}	Power	Supply Voltage for Internal Analog Circuits
15	AIN	Input	Ambient Light Sensor Input
16	AREF	Output	Reference Voltage for Ambient Light Sensor, 1.23V
17	GND_T	Ground	Ground
18	V_{REF}	Output	Internal Reference Bypass Capacitor
19	RT	Input	Oscillator Resistor
20	MW_SEL	Logic Input	MicroWire — I^2C select (MW_SEL=1 in MicroWire Mode)

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Pin Description (continued)

Pin	Name	Type	Description
21	NRST	Logic Input	Low Active Reset Input
22	CS	Logic Input/Output	MicroWire Chip-Select (in) / I^2C SDA (in/out)
23	DO	Logic Output	MicroWire Data Output
24	DI	Logic Input	MicroWire Data Input
25	SCL	Logic Input	MicroWire Clock / I^2C SCL Input
26	RGB_EN	Logic Input	LED Control for On/Off or PWM Dimming
27	V_{DD_IO}	Power	Supply Voltage for Logic IO signals
28	ROUT	LED Output	Open Drain Output, Red LED
29	GOUT	LED Output	Open Drain Output, Green LED
30	BOUT	LED Output	Open Drain Output, Blue LED
31	GND_RGB	Ground	Ground for RGB Drivers
32	OUT	Output	Open Drain, Boost Converter Power Switch

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2][3]

V_{DD1}, V_{DD2}, V_{DD_IO}, V(OUT, FB)	-0.3V to 6.0V
Voltage on Logic Pins	-0.3V to V_{DD_IO} + 0.3V, with 6.0V max
Voltage on LED Output Pins	-0.3V to V(FB) + 0.3V, with 6.0V max
Voltage on All Other Pins	-0.3V to $V_{DD1,2}$ + 0.3V, with 6.0V max
I (ROUT, GOUT, BOUT)	150 mA
I (V_{REF})	10 µA
Continuous Power Dissipation[4]	Internally Limited
Junction Temperature ($T_{J\text{-}MAX}$)	125°C
Storage Temperature Range	−65°C to +150°C
Maximum Lead Temperature (Reflow soldering, 3 times)[5]	260°C
ESD Rating[6]	
Human Body Model:	2 kV
Machine Model:	200V

(1) All voltages are with respect to the potential at the GND pins (GND1, GND2, GND_T, GND_BOOST, GND_WLED, GND_RGB).
(2) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply performance limits. For performance limits and associated test conditions, see the Electrical Characteristics table.
(3) **If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office / Distributors for availability and specifications.**
(4) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 160°C (typ.) and disengages at T_J = 140°C (typ.).
(5) **For detailed soldering specifications and information, see TI's AN--1125 Application Report (SNAA002)**.
(6) The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin. MIL-STD-883 3015.7

Operating Ratings[1][2]

V_{DD1}, V_{DD2}	3.0V to 6.0V
V_{DD_IO}	1.65V – $V_{DD1,2}$
Recommended Load Current	0 mA to 250 mA
Junction Temperature (T_J) Range	−40°C to +125°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply performance limits. For performance limits and associated test conditions, see the Electrical Characteristics table.
(2) All voltages are with respect to the potential at the GND pins (GND1, GND2, GND_T, GND_BOOST, GND_WLED, GND_RGB).

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Operating Ratings[1][2] (continued)

Ambient Temperature (T_A) Range[3]	−40°C to +85°C

(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation:
$T_{A-MAX} = T_{J-MAX-OP} - (\theta_{JA} \times P_{D-MAX})$.

Thermal Characteristics

Junction-to-Ambient Thermal Resistance (θ_{JA}),	
NPC0032A Package [1]	72°C/W

(1) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

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Electrical Characteristics [1] [2]

Limits in standard typeface are for T_J = 25°C. Limits in **boldface** type apply over the operating ambient temperature range (−40°C ≤ T_A ≤ +85°C). Unless otherwise noted, specifications apply to the Block Diagram with: V_{DD1} = V_{DD2} = V_{DD_IO} = 3.6V, C_{VDD1}, C_{VDD2}, C_{VDDIO} = 1 µF, C_{IN}, C_{OUT} = 10 µF, C_{VDDA} = 1 µF, C_{VREF} = 0.1 µF, L_{BOOST} = 10 µH [3].

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{DD1,2}$	Supply Voltage		3.0	3.6	6.0	V
I_{DD}	Standby Supply Current (V_{DD1} and V_{DD2} current)	NSTBY = L (register) CS, SCL, DI, NRST = H V_{DD1}, V_{DD2} = 3.6V		1	**7**	µA
	No-Load Supply Current (V_{DD1} and V_{DD2} current, boost off)	NSTBY = H (reg.) EN_BOOST = L (reg.) SCL, CS, DI, NRST = H		170	**300**	µA
	Full Load Supply Current (V_{DD1} and V_{DD2} current, boost on)	NSTBY = H (register) NRST, CS, SCL, DI = H RGB_EN = L WLED1 … 6 = L EN_AMBADC = L		1		mA
I_{DD_IO}	V_{DD_IO} Standby Supply Current	NSTBY = L (register) CS, SCL, DI, NRST = H		1		µA
	V_{DD_IO} Operating Supply Current	1 MHz Clock Frequency C_L = 50 pF at DO pin		20		µA
V_{REF}	Reference Voltage [4]	I_{REF} ≤ 1 nA, Test Purposes Only	**1.205** **−2**	1.23	**1.255** **+2**	V %
V_{DDA}	LDO Output Voltage	IV_{DDA} < 1 µA	**2.688** **–4**	2.8	**2.912** **+4**	% V

(1) All voltages are with respect to the potential at the GND pins (GND1, GND2, GND_T, GND_BOOST, GND_WLED, GND_RGB).
(2) Min and Max limits are specified by design, test, or statistical analysis. Typical numbers represent the most likely norm.
(3) Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) are used in setting electrical characteristics.
(4) V_{REF} pin (Bandgap reference output) is for internal use only. A capacitor should always be placed between V_{REF} and GND1.

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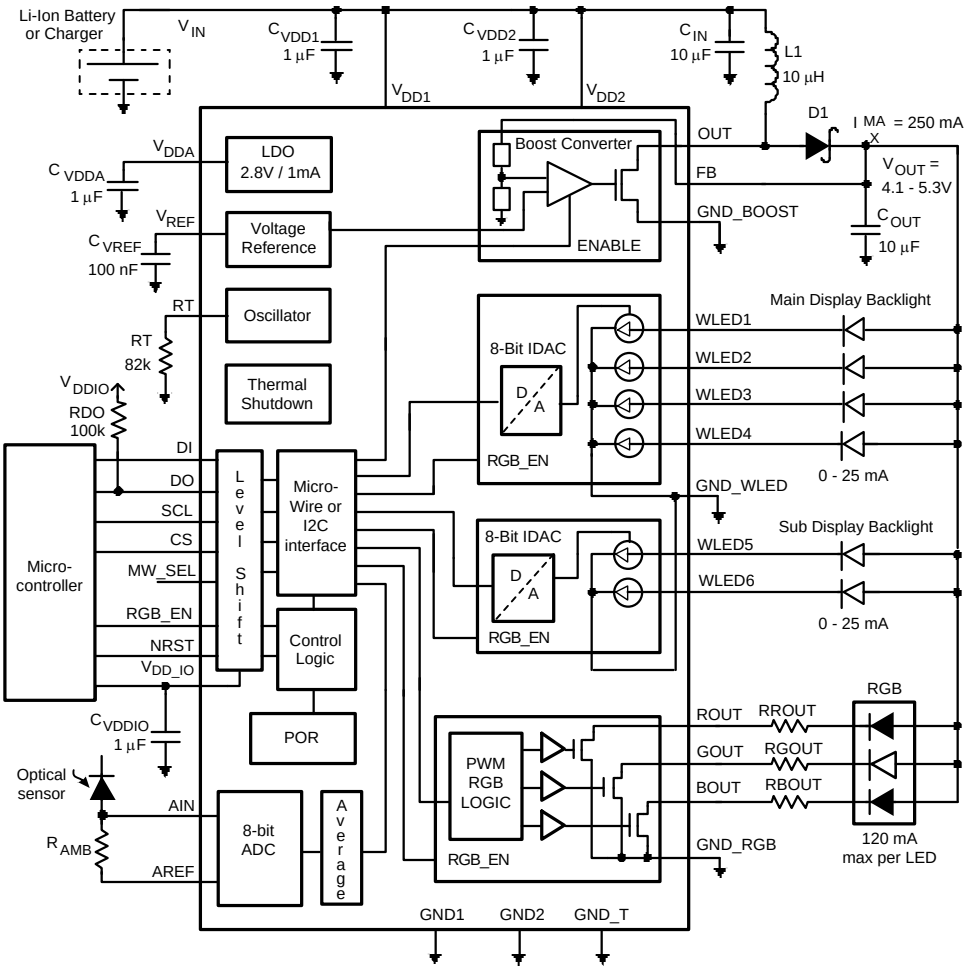
BLOCK DIAGRAM



Modes of Operation

RESET: In the RESET mode all the internal registers are reset to the default values. Boost output register is set to 4.55V (register 0Dh = 07h), ext_pwm is enabled for color outputs (register 2Bh = 1Ch), EN_BOOST bit is high (register 0Bh bit 5) and all other registers are set to 00h. Reset is entered always if input NRST is LOW or internal Power On Reset is active.

STANDBY: The STANDBY mode is entered if the register bit NSTBY is LOW and Reset is not active. This is the low power consumption mode, when all circuit functions are disabled. Registers can be written in this mode and the control bits are effective immediately after start up.

STARTUP: INTERNAL STARTUP SEQUENCE powers up all the needed internal blocks (V_{REF}, Bias, Oscillator, etc.). To ensure the correct oscillator initialization, a 10 ms delay is generated by the internal state-machine. Thermal shutdown (THSD) disables the chip operation and Startup mode is entered until *no* thermal shutdown event is present.

BOOST STARTUP: Soft start for boost output is generated in the BOOST STARTUP mode. In this mode the boost output is raised in PFM mode during the 10 ms delay generated by the state-machine. The Boost startup is entered from Internal Startup Sequence if EN_BOOST is HIGH or from Normal mode when EN_BOOST is written HIGH. During Boost Startup all LEDs are turned off to reduce the loading.

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NORMAL: During NORMAL mode the user controls the chip using the *Control Registers*. The registers can be written in any sequence and any number of bits can be altered in a register in one write.

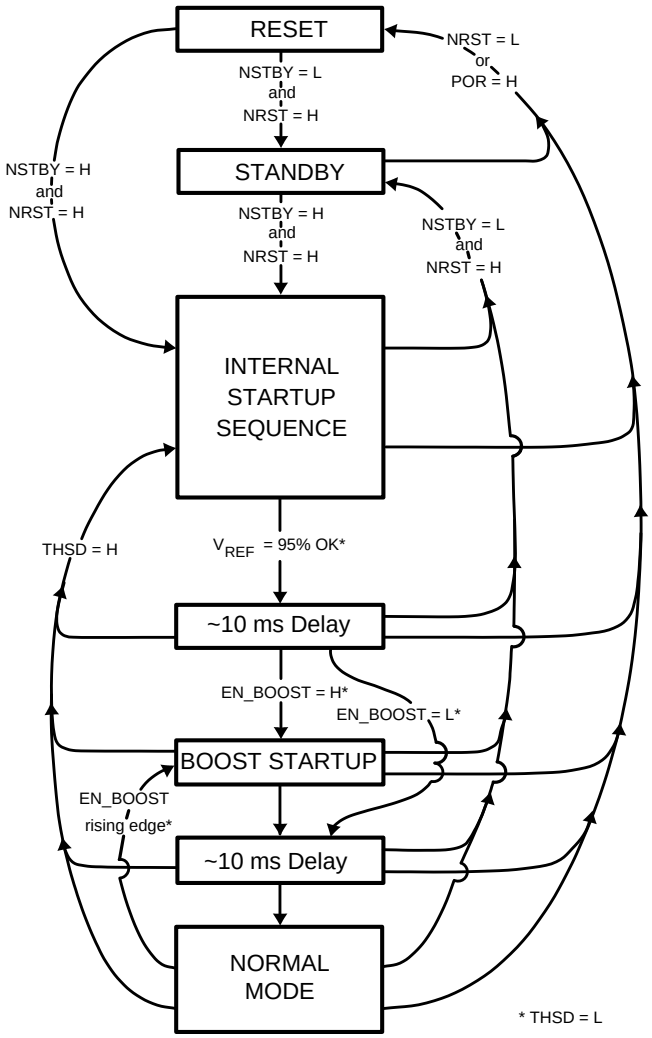

Figure 3. Modes of Operation Flowchart

Logic Interface Characteristics ($1.8V \le V_{DD_IO} \le V_{DD1,2}$)(5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LOGIC INPUTS DI, SCL, NRST, RGB_EN, CS, MW_SEL						
V_{IL}	Input Low Level				**0.5**	V
V_{IH}	Input High Level		**V_{DD_IO} − 0.5**			V
I_I	Logic Input Current		**−1.0**		**1.0**	µA
f_{SCL}	Clock Frequency	I^2C Mode			**400**	kHz
		MicroWire Mode			**8**	MHz
LOGIC OUTPUTS DO, CS						
V_{OL}	Output Low Level	$I_{DO,\ CS}$ = 3 mA		0.3	**0.6**	V
V_{OH}	Output High Level	I_{DO} = − 3 mA	**V_{DD_IO} − 0.6**	V_{DD_IO} − 0.3		V
I_L	Output Leakage Current	V_{DO} = 2.8V			**1.0**	µA

(5) In I^2C mode operating ratings are limited to $3.0V \le V_{DD1,2} \le 4.5V$ and $-20°C \le T_A \le +85°C$.

Logic Interface Characteristics (1.65V ≤ V_{DD_IO} ≤ 1.8V) (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LOGIC INPUTS DI, SCL, NRST, RGB_EN, CS, MW_SEL						
V_{IL}	Input Low Level				**0.35**	V
V_{IH}	Input High Level		**V_{DD_IO} − 0.35**			V
I_I	Logic Input Current		**−1.0**		**1.0**	µA
f_{SCL}	Clock Frequency	I^2C Mode			**200**	kHz
		MicroWire Mode			**4**	MHz
LOGIC OUTPUTS DO, CS						
V_{OL}	Output Low Level	$I_{DO, CS}$ = 2mA		0.3	**0.6**	V
V_{OH}	Output High Level	I_{DO} = − 2mA	**V_{DD_IO} − 0.6**	V_{DD_IO} − 0.3		V
I_L	Output Leakage Current	V_{DO} = 2.8V			**1.0**	µA

(1) In I^2C mode operating ratings are limited to 3.0V ≤ $V_{DD1,2}$ ≤ 4.5V and –20°C ≤ T_A ≤ +85°C.

Control Interface

The LP3936 supports two different interfaces modes:

1) MicroWire/SPI interface

2) I^2C compatible interface

User can define the interface by MW_SEL pin. The pin configuration will also change depending on which interface is selected. The following table shows the selections for both interface modes.

MW_SEL	Interface	Pin Configuration		Comment
1	MicroWire/SPI	SCL DI DO CS	(clock) (data in) (data out) (chip select)	
0	I^2C Compatible	SCL CS = SDA	(clock) (data in/out)	Use pull up resistor for SCL Use pull up resistor for SDA

MicroWire/SPI Interface

The Microwire transmission consists of 16-bit Write and Read Cycles. One cycle consists of 7 Address bits, 1 Read/Write (R/W) bit and 8 Data bits. Read is done in two cycles: address is provided in the first cycle and the data is sent out on the next cycle. R/W bit high state defines a Write Cycle and low defines a Read Cycle. DO output is normally in high-impedance state and it is active only during Write and Read Cycles. A pull-up or pull-down resistor may be needed in DO line if a floating logic signal can cause unintended current consumption in other circuits where DO is connected.

The Address and Data are transmitted MSB first. The Chip Select signal CS must be low during the Cycle transmission. CS resets the interface when high and it has to be taken high between successive Cycles. Data is clocked in on the rising edge of the SCL clock signal, while data is clocked out on the falling edge of SCL.

The MicroWire interface mode can also support SPI interface. The difference with normal SPI interface is that in LP3936 the Read operation from a new address needs two read cycles. If repetitive reads are made from the same address, a correct value is obtained on every read cycle.

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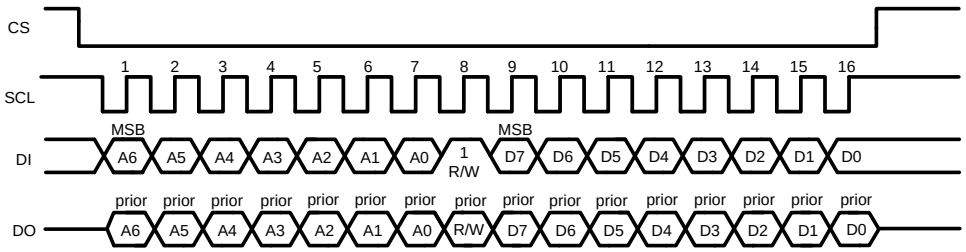


Figure 4. MicroWire Write Cycle

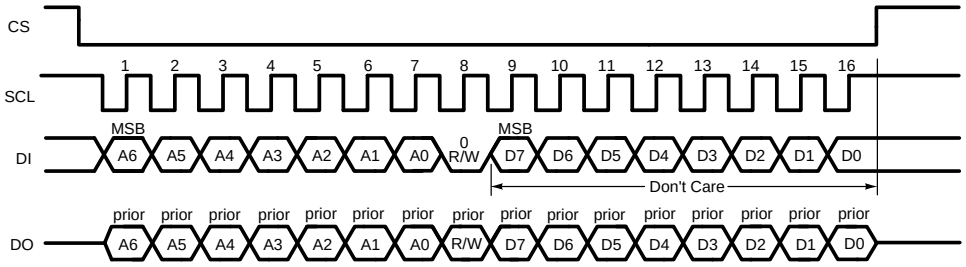


Figure 5. MicroWire Read Cycle 1

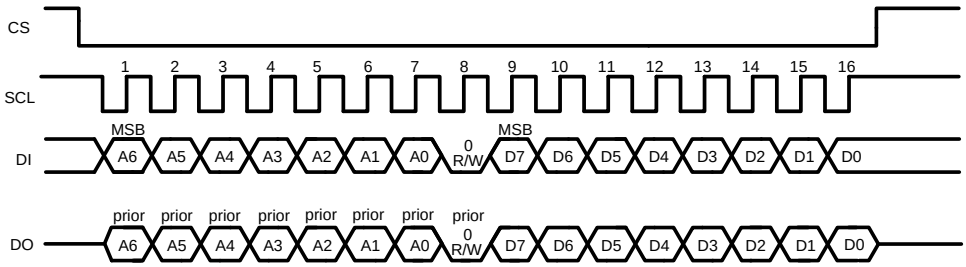


Figure 6. MicroWire Read Cycle 2

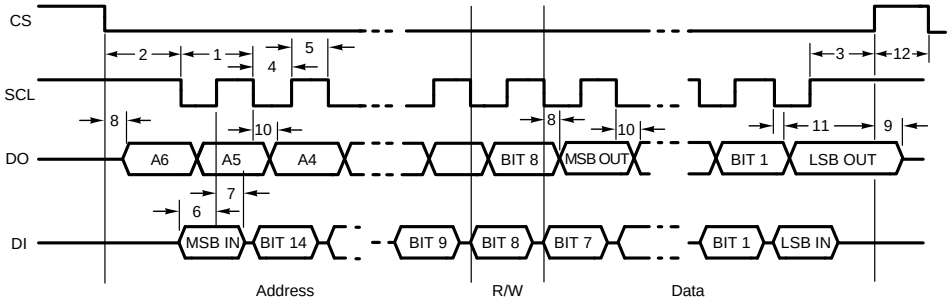


Figure 7. MicroWire Timing Diagram

MicroWire Timing Parameters(1)

$V_{DD1,2}$ = 3.0V – 6V, V_{DD_IO} = 1.8V – $V_{DD1,2}$

Symbol	Parameter	Limit		Units
		Min	Max	
1	Cycle Time	120		ns
2	Enable Lead Time	60		ns
3	Enable Lag Time	60		ns
4	Clock Low Time	60		ns
5	Clock High Time	60		ns
6	Data Setup Time	0		ns
7	Data Hold Time	10		ns
8	Data Access Time		35	ns
9	Disable Time		30	ns
10	Output Data Valid		55	ns
11	Output Data Hold Time	15		ns
12	CS Inactive Time	10		ns

(1) Specified by design. Not production tested.

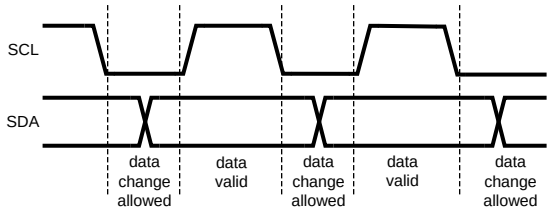
I²C Compatible Interface

I²C SIGNALS

In I²C mode the LP3936 pin SCL is used for the I²C clock and the pin CS is used for the I²C data signal SDA. Both these signals need a pull-up resistor according to I²C specification. Unused pin DO can be left unconnected and pin DI must be connected to V_{DD_IO} or GND.

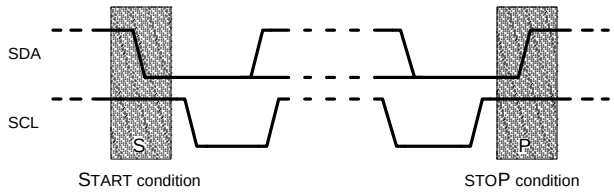
I²C DATA VALIDITY

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when CLK is LOW.



I²C START AND STOP CONDITIONS

START and STOP bits classify the beginning and the end of the I²C session. START condition is defined as SDA signal transitioning from HIGH to LOW while SCL line is HIGH. STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates START and STOP bits. The I²C bus is considered to be busy after START condition and free after STOP condition. During data transmission, I²C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.



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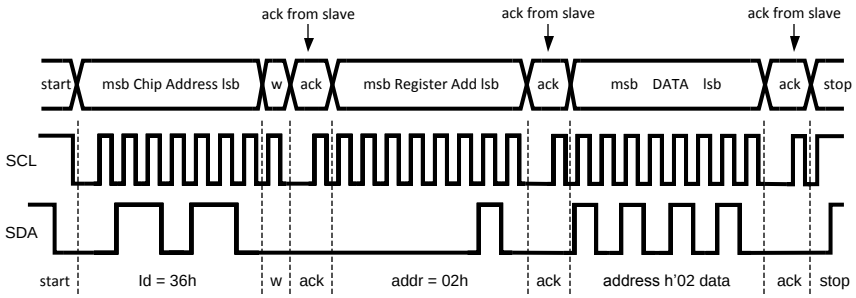
TRANSFERRING DATA

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the 9th clock pulse, signifying an acknowledge. A receiver which has been addressed must generate an acknowledge after each byte has been received.

After the START condition, the I^2C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The LP3936 address is 36h. For the eighth bit, a “0” indicates a WRITE and a “1” indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

Figure 8. I^2C Chip Address



w = write (SDA = “0”)
r = read (SDA = “1”)
ack = acknowledge (SDA pulled down by either master or slave)
rs = repeated start
id = chip address, 36h for LP3936

Figure 9. I^2C Write Cycle

When a READ function is to be accomplished, a WRITE function must precede the READ function, as shown in the Read Cycle Waveform.

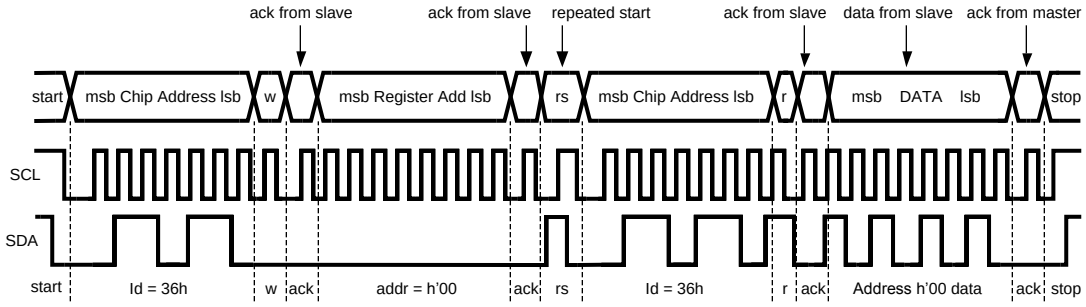


Figure 10. I^2C Read Cycle

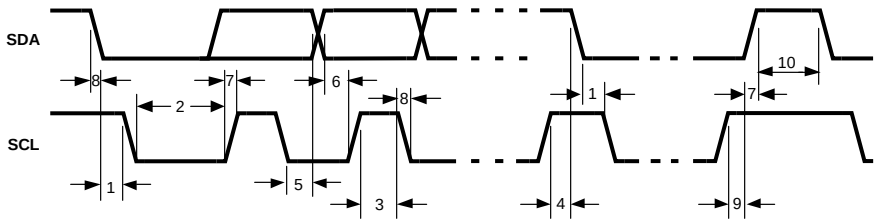


Figure 11. I²C Timing Diagram

I²C Timing Parameters(1)

$V_{DD1,\ 2}$ = 3.0V to 4.5V, V_{DD_IO} = 1.65V to $V_{DD1,\ 2}$

Symbol	Parameter	Limits		Units
		Min	Max	
1	Hold Time (repeated) START Condition	0.6		µs
2	Clock Low Time	1.3		µs
3	Clock High Time	600		ns
4	Setup Time for a Repeated START Condition	600		ns
5	Data Hold Time (output direction, delay generated by LP3936)	300	900	ns
5	Data Hold Time (input direction)	0	900	ns
6	Data Setup Time	100		ns
7	Rise Time of SDA and SCL	20 + 0.1C_b	300	ns
8	Fall Time of SDA and SCL	15 + 0.1C_b	300	ns
9	Set-Up Time for STOP Condition	600		ns
10	Bus Free Time between a STOP and a START Condition	1.3		µs
C_b	Capacitive Load for Each Bus Line	10	200	pF

(1) Specified by design. Not production tested.

A/D Converter for Ambient Light Measurement

Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{IN\ RANGE}$	Input Voltage	AD Output: 00h		1.23		V
		AD Output: FFh		2.46		V
DNL	Differential Non-Linearity		–1.5	±1	+1.5	LSB
GE	Gain Error		−5		+5	LSB
PSS	Power Supply Sensitivity	3.1V ≤ V_{DD} ≤ 4.2V		±1/2		LSB
f(conv)	Conversion Rate	Without Averaging		217		Hz
		With Averaging (64 samples)		3.4		Hz
$t_{STARTUP}$	Startup Time			100		ms
I_{AIN}	Input Current	1.23 < AIN < 2.6V		±0.1		µA
I_{AREF}	Maximum Output Current	AREF Output Current Sink		200		µA
R_{AREF}	AREF Output Resistance			110		Ω

ADC output AIN[7:0] can be read from address 0CH after startup time. Overflow bit can be read from bit D7 in address 0BH. The overflow bit indicates that input voltage exceeds the input voltage range of the ADC. The ADC output value in this case is FFH. When averaging is on, the overflow is high, if any of the 64 conversion results in the averaging period overflows. Thus the averaged result may be considerably below maximum and the overflow can still be high, if the input signal is noisy.

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Examples for optical sensor are photodiode SHF2400 and phototransistor SFH3410 from Osram or BSC 3216 G1 optical sensor from TDK.

ADC can be used for temperature measurement with a thermistor. It enables temperature compensated LED driving.

If ADC is not used, it should be disabled by writing en_ambadc bit low. AIN and AREF pins can be left unconnected.

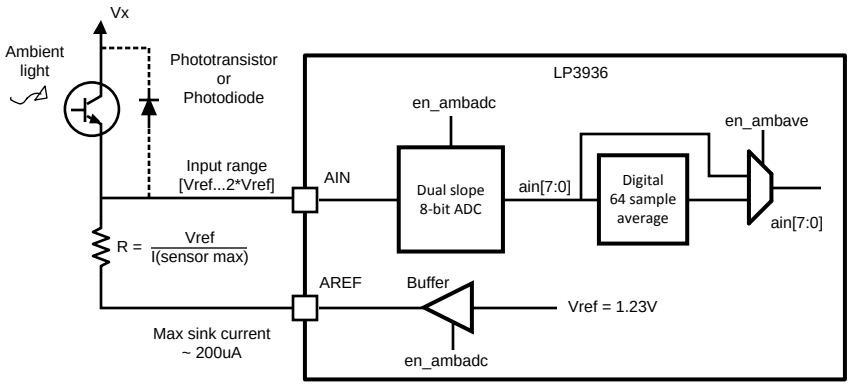

Figure 12. A/D Converter – Ambient Light Measurement Circuitry

Magnetic Boost DC/DC Converter

The LP3936 Boost DC/DC Converter generates a 4.1V–5.3V supply voltage for the LEDs from single Li-Ion battery (3V … 4.5V). The output voltage is controlled with an 8-bit register in 9 steps. The converter is a magnetic switching PFM/PWM mode DC/DC converter with a current limit. The converter has a 1 MHz switching frequency when timing resistor RT is 82 kΩ.

The topology of the magnetic boost converter is called CPM control, current programmed mode, where the inductor current is measured and controlled with the feedback. The user can program the output voltage of the boost converter. The control changes the resistor divider in the feedback loop.

Figure 13 shows the boost topology with the protection circuitry. Three different protection schemes are implemented:

1) Over voltage protection, limits the maximum output voltage
   a. Keeps the output below breakdown voltage.
   b. Prevents boost operation if battery voltage is much higher than desired output.
2) Over current protection, limits the maximum inductor current
   a. Voltage over switching NMOS is monitored; too high voltages turn the switch off.
3) Duty cycle limiting, done with digital control.

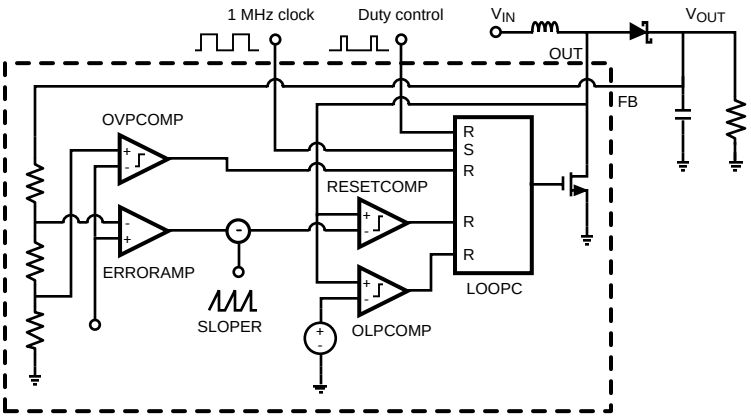

Figure 13. Magnetic Boost DC/DC Converter – Boost Topology with Protection Circuitry

Boost Output Voltage Control

User can control the boost output voltage by boost output 8-bit register.

8-Bit Boost Output Voltage Control Register Description

Boost[7:0] Register 0Dh		BOOST Output Voltage (typical)
Binary	**Hex**	
0000 0000	00	4.10
0000 0001	01	4.25
0000 0011	03	4.40
0000 0111	**07**	**4.55 Default**
0000 1111	0F	4.70
0001 1111	1F	4.85
0011 1111	3F	5.00
0111 1111	7F	5.15
1111 1111	FF	5.30

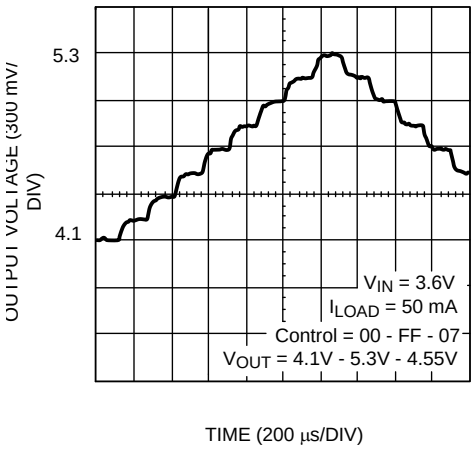

Figure 14. Boost Output Voltage Control

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Magnetic Boost DC/DC Converter Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LOAD}	Load Current	3.0V ≤ V_{IN} ≤ 4.5V V_{OUT} = 4.55V	0		250	mA
V_{OUT}	Output Voltage Accuracy (FB Pin)	1 mA ≤ I_{LOAD} ≤ 225 mA 3.0V ≤ V_{IN} ≤ V (FB)−0.5V V_{OUT} = 4.55V	**−5**		**+5**	%
	Output Voltage (FB Pin)	1 mA ≤ I_{LOAD} ≤ 250 mA 3.0V < V_{IN} < 4.55V + $V_{(SCHOTTKY)}$		4.55		V
		1 mA ≤ I_{LOAD} ≤ 250 mA V_{IN} > 4.55V + $V_{(SCHOTTKY)}$		V_{IN}–$V_{(SCHOTTKY)}$		V
RDS_{ON}	Switch ON Resistance	$V_{DD1,2}$ = 3.6V, I_{SW} = 0.5A		0.4	**0.5**	Ω
f_{PWF}	PWM Mode Switching Frequency	RT = 82 kΩ		1		MHz
	Frequency Accuracy	RT = 82 kΩ	−6	±3	+6	%
			−10		**+10**	
$t_{STARTUP}$	Startup Time			25		ms
I_{CL_OUT}	OUT Pin Current Limit	V_{DD} = 3.6V	600	750	1050	mA
			400		**1200**	

PFM/PWM Mode

User can change the Boost converters mode between PWM (Pulse Width Modulation) and PFM (Pulse Frequency Modulation). The startup is done on PFM mode and then the device runs on PWM mode (as a default). User can set PFM mode by turning “pfm_mode” register bit HIGH. PFM is recommended to use with light loads and PWM with high loads.

Boost Standby Mode

User can set boost converter to STANDBY mode by writing register bit EN_BOOST low. This mode can be useful when driving LEDs directly from battery voltage. This may be possible if LED forward voltage is low, battery voltage is high and LED current is low.

When EN_BOOST is written high, the converter starts for 10 ms in PFM mode and then goes to PWM mode if PWM mode has been selected (default). During Boost Start-up all LEDs are turned off to reduce the load.

Unused Boost Converter

If the boost converter is not used, it should be disabled by writing bit en_boost low. OUT pin should be connected to GND and FB pin to the LED supply voltage.

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BOOST CONVERTER TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.6V, V_{OUT} = 4.55V if not otherwise stated.

Boost Converter Efficiency (R_{OUT}, G_{OUT}, B_{OUT} outputs)

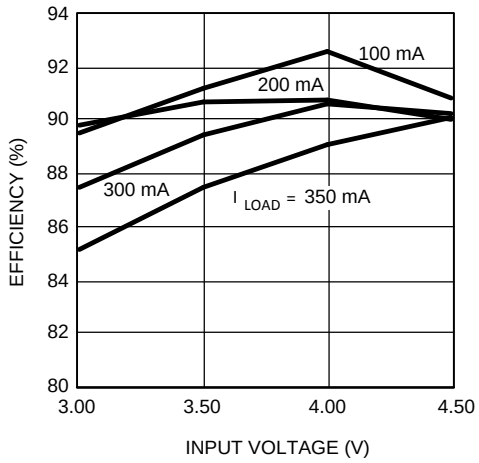

Figure 15.

Boost Frequency vs RT Resistor

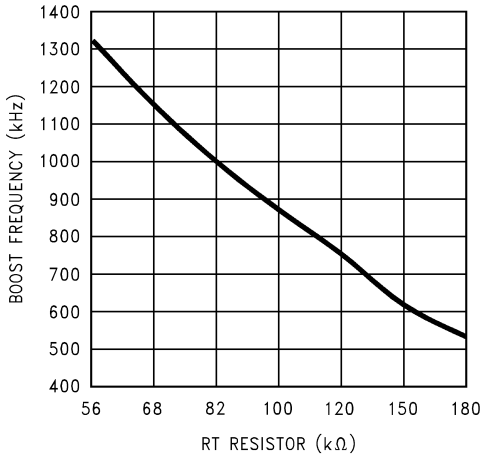

Figure 16.

Battery Current vs Voltage

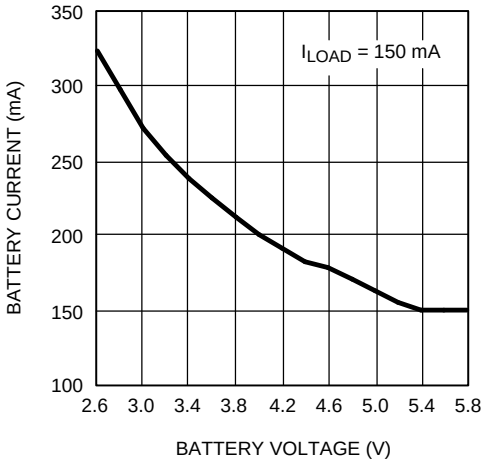

Figure 17.

Battery Current vs Voltage

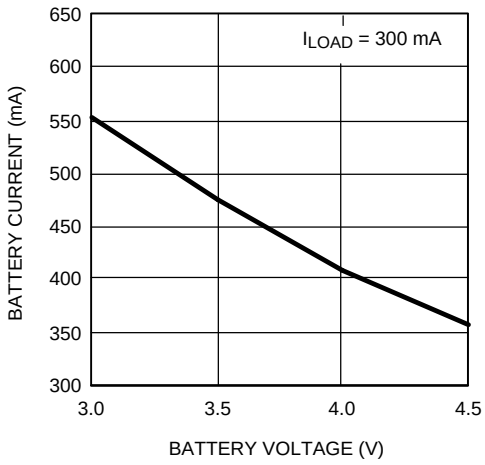

Figure 18.

Boost Typical Waveforms at 100 mA Load

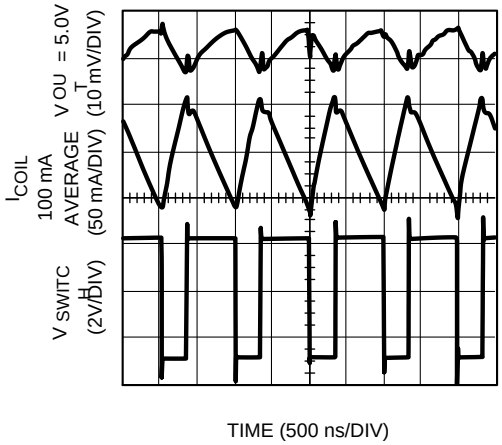

Figure 19.

Boost Startup with No Load

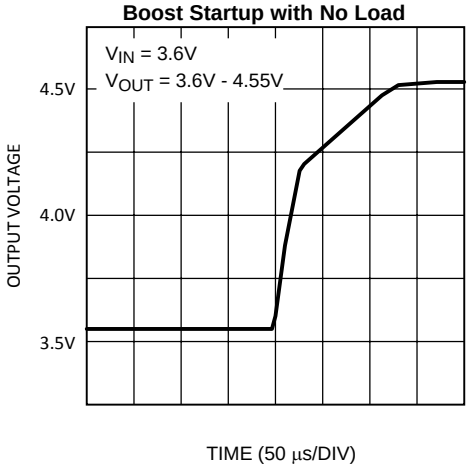

Figure 20.

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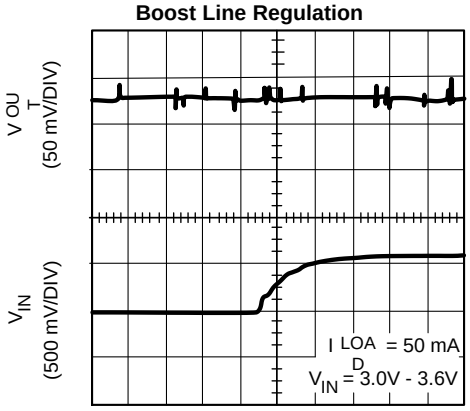
BOOST CONVERTER TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 3.6V, V_{OUT} = 4.55V if not otherwise stated.

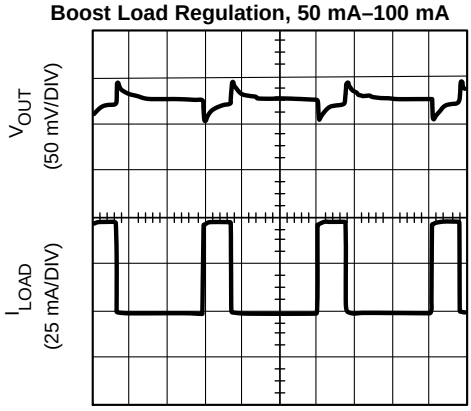
Boost Line Regulation



TIME (100 µs/DIV)

Figure 21.

Boost Load Regulation, 50 mA–100 mA



TIME (50 µs/DIV)

Figure 22.

APPLICATION INFORMATION

RGB LED Driver

The RGB driver has three outputs that can independently drive one RGB LED or three LEDs of any kind. User has control over the following parameters separately for each LED:

- **ON and OFF** (start and stop time in blinking cycle)
- **DUTY** (PWM brightness control)
- **SLOPE** (dimming slope)
- **ENABLE** (direct enable control)

The main blinking cycle is controlled with 2-bit CYCLE control (0.25 / 0.5 / 1.0 / 2.0s).

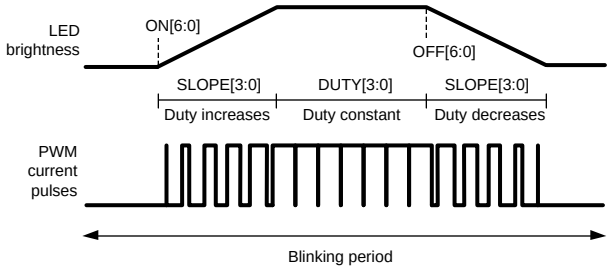


Figure 23. RGB PWM Operating Principle

RGB_START is the master enable control for the whole RGB function. The internal PWM and blinking control can be disabled by setting the RGB_PWM control LOW. In this case the individual enable controls can be used to switch outputs on and off. RGB_EN input can be used for external hardware PWM control. RGB_EN input can be used as direct on/off or brightness (PWM) control. If RGB_EN input is not used, it must be tied to V_{DD_IO}. Recommended maximum frequency of RGB LED external PWM control is 1 MHz.

In the normal PWM mode the R, G and B switches are controlled in 3 phases (one phase per driver). During each phase the peak current set by external resistor is driven through the LED for the time defined by DUTY setting (0 µs–50 µs). As a time averaged current this means 0%–33% of the peak current. The PWM period is 150 µs and the pulse frequency is 6.67 kHz in normal mode.

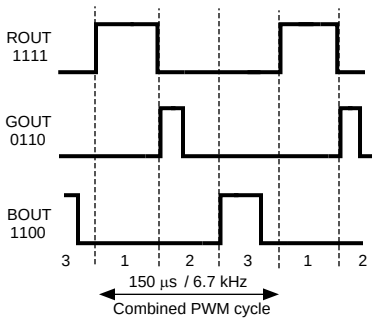


Figure 24. Normal Mode PWM Waveforms at different duty settings

In the FLASH mode all the outputs are controlled in one phase and the PWM period is 50 µs. The time averaged FLASH mode current is three times the normal mode current at the same DUTY value.

Blinking can be controlled separately for each output. On and OFF times determine, when a LED turns on and off within the blinking cycle. When both ON and OFF are 0, the LED is on and doesn't blink. If ON equals OFF but is not 0, the LED is permanently off.

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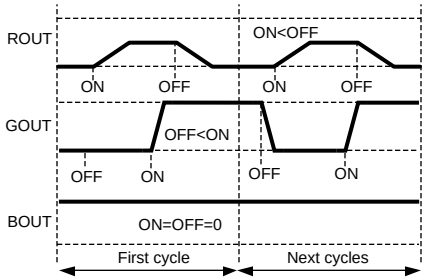

Figure 25. Example Blinking Waveforms

RGB Driver Electrical Characteristics

(R_{OUT}, G_{OUT}, B_{OUT} outputs)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
R_{DS-ON}	ON Resistance			2	**4.5**	Ω
$I_{LEAKAGE}$	Off State Leakage Current	V_{FB} = 5.3V		0.04	**1**	µA
I_{MAX}	Maximum Sink Current	See (1)			**120**	mA
T_{SMAX}	Maximum Slope Period	Maximum Duty Setting		0.93		s
T_{SMIN}	Minimum Slope Period	Maximum Duty Setting		31		ms
T_{SRES}	Slope Resolution	Maximum Duty Setting		62		ms
$T_{START/STOP}$	Start/Stop Resolution	Cycle 1s		1/16		s
Duty	Duty Step Size			1/16		
T_{BLINK}	Blinking Cycle Accuracy		−6	±3	+6	%
D_{CYCF}	Duty Cycle Range	EN_FLASH = 1	0		94	%
D_{CYC}	Duty Cycle Range	EN_FLASH = 0	0		31	%
D_{RESF}	Duty Resolution	EN_FLASH = 1 (4-bit)		6.27		%
D_{RES}	Duty Resolution	EN_FLASH = 0 (4-bit)		2.09		%
F_{PWMF}	PWM Frequency	EN_FLASH = 1		20		kHz
F_{PWM}	PWM Frequency	EN_FLASH = 0		6.67		kHz

(1) The total load current of the boost converter should be limited to 250 mA.

RGB LED PWM Control(2)

RDUTY[3:0] GDUTY[3:0] BDUTY[3:0]	DUTY sets the brightness of the LED by adjusting the duty cycle of the PWM driver. The minimum DUTY cycle [0000] is 0% and the maximum [1111] in the Flash mode is 94% and in the normal mode 31% of the peak pulse current. The peak pulse current is determined by the external resistor, LED forward voltage drop and the boost voltage.
RSLOPE[3:0] GSLOPE[3:0] BSLOPE[3:0]	SLOPE sets the turn-on and turn-off slopes. Fastest slope is set by [0000] and slowest by [1111]. SLOPE changes the duty cycle at constant, programmable rate. For each slope setting the maximum slope time appears at maximum DUTY setting. When DUTY is reduced, the slope time decreases proportionally. For example, in case of maximum DUTY, the sloping time can be adjusted from 31 ms [0000] to 930 ms [1111]. For 50% DUTY [1000] the sloping time is 17 ms [0000] to 496 ms [1111]. The blinking cycle has **no** effect on SLOPE.
RON[6:0] GON[6:0] BON[6:0]	ON sets the beginning time of the turn-on slope. The on-time is relative to the selected blinking cycle length. On-setting N (N = 0–127) sets the on-time to N/128 * cycle length.
ROFF[6:0] GOFF[6:0] BOFF[6:0]	OFF sets the beginning time of the turn-off slope. Off-time is relative to blinking cycle length in the same way as on-time.
	If **ON = 0, OFF = 0** and **RGB_PWM = 1**, then RGB outputs are continuously on (no blinking), DUTY controls the brightness and SLOPE is ignored. **If ON and OFF are the same, but not 0, RGB outputs are turned off.**

(2) TI's *AN-1293 Driving RGB LEDs Using LP3936 Lighting Management System Application Report* (SNVA071) contains a thorough description of the RGB driver functionality including programming examples.

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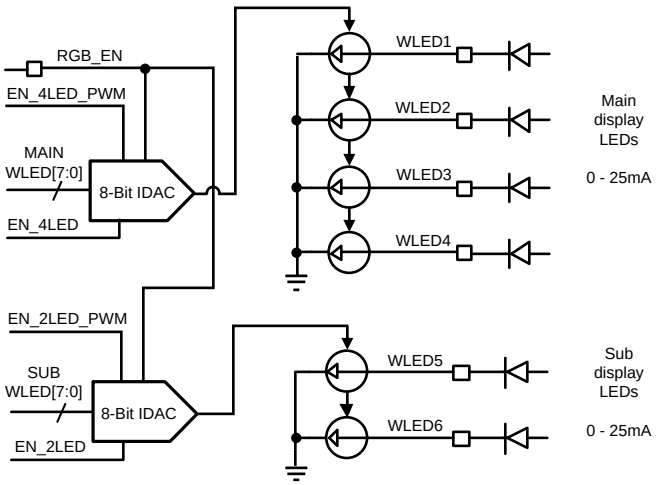
CYCLE[1:0]	CYCLE sets the blinking cycle: [00] for 0.25s, [01] for 0.5s, [10] for 1s and [11] for 2s. CYCLE setting is common to all R, G and B drivers.
RSW GSW BSW	Enable for R switch Enable for G switch Enable for B switch
RGB_START	Master Switch: RGB_START = 0 → RGB OFF RGB_START = 1 → RGB ON, starts the new cycle from t = 0
RGB_PWM	RGB_PWM = 0 → RSW, GWS and BSW control directly the RGB outputs (on/off control only) RGB_PWM = 1 → Normal PWM RGB functionality (duty, slope, on/off times, cycle)
EN_FLASH	Flash Mode enable control for RGB. In Flash mode (EN_FLASH = 1) RGB outputs are PWM controlled simultaneously, not in 3-phase system as in the Normal Mode.
EN_RED_PWM EN_GREEN_PWM EN_BLUE_PWM	EN_X_PWM = 0 → External PWM control from RGB_EN pin is disabled EN_X_PWM = 1 → External PWM control from RGB_EN pin is enabled Internal PWM control (DUTY) can be used independently of external PWM control. External PWM has the same effect on all enabled colors.

WLED Drivers

White LED drivers drive each white LED with a regulated constant current. The outputs are combined in two groups, four outputs for the main display backlight and two outputs for the sub display backlight. The current is controlled between 0 and 25.5 mA using the 8-bit current mode DA-converters. WLED outputs can be used to drive any kind of LED.

Main and sub display outputs have separate enable control bits, EN_4LED and EN_2LED.

PWM control of WLED outputs for dimming or on/off control is possible using RGB_EN pin together with EN_4LED_PWM and EN_2LED_PWM enable control bits from the user register. Recommended maximum frequency of WLED external PWM control is 1 kHz.



WLED and CLED Driver Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{RANGE}	Sink Current Range	V_{FB} = 4.55V, Control 00h–FFh		0–25.5		mA
I_{MAX}	Maximum Sink Current	See (1)	24	25.5	27	mA
			22		**28**	mA
$I_{LEAKAGE}$	Leakage Current	V_{FB} = 5V		0.04	**1**	µA
I_{MATCH}	Sink Current Matching (2)	I_{SINK} = 13 mA, between WLED1 … 4 or WLED5 … 6		1.0	**4**	%

(1) A minimum voltage, Dropout Voltage, is required on the WLED outputs for maintaining the LED current. The current reduction at lower voltages is shown by the graph in Figure 26.
(2) Match % = 100% * (Max – Min)/Min

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WLED Current Adjustment

WLED[7:0]	WLED Current (Typical)	Units
0000 0000	0	mA
0000 0001	0.1	mA
0000 0010	0.2	mA
0000 0011	0.3	mA
•	•	•
•	•	•
1111 1101	25.3	mA
1111 1110	25.4	mA
1111 1111	25.5	mA

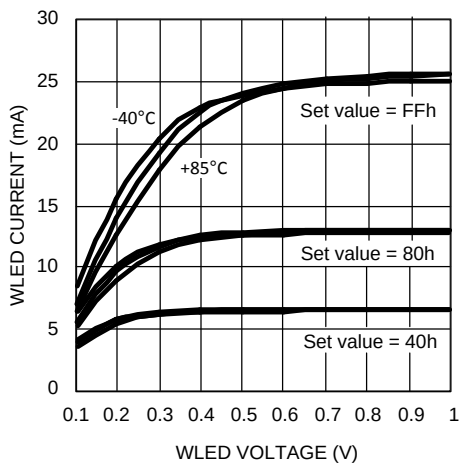

Figure 26. WLED Output Current vs Voltage Temperatures −40°C, +25°C, +85°C

Recommended External Components

OUTPUT CAPACITOR, C_{OUT}

The output capacitor C_{OUT} directly affects the magnitude of the output ripple voltage. In general, the higher the value of C_{OUT}, the lower the output ripple magnitude. Multilayer ceramic capacitors with low ESR are the best choice. At the lighter loads, the low ESR ceramics offer a much lower V_{OUT} ripple than the higher ESR tantalums of the same value. At the higher loads, the ceramics offer a slightly lower V_{OUT} ripple magnitude than the tantalums of the same value. However, the dv/dt of the V_{OUT} ripple with the ceramics is much lower than the tantalums under all load conditions. Capacitor voltage rating must be sufficient, 10V is recommended. It should be noted that with some capacitor types the actual capacitance depends heavily on the capacitor DC voltage bias.

INPUT CAPACITOR, C_{IN}

The input capacitor C_{IN} directly affects the magnitude of the input ripple voltage and to a lesser degree the V_{OUT} ripple. A higher value C_{IN} will give a lower V_{IN} ripple. Capacitor voltage rating must be sufficient, 10V is recommended.

OUTPUT DIODE, D_{OUT}

A Schottky diode should be used for the output diode. To maintain high efficiency the average current rating of the schottky diode should be larger than the peak inductor current (1A). Schottky diodes with a low forward drop and fast switching speeds are ideal for increasing efficiency in portable applications. Choose a reverse breakdown of the schottky diode larger than the output voltage. Do not use ordinary rectifier diodes, since slow switching speeds and long recovery times cause the efficiency and the load regulation to suffer.

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INDUCTOR, L

The high switching frequency enables the use of the small surface mount inductor. A 10 µH shielded inductor is suggested. Values below 4.7 µH should not be used. The inductor should have a saturation current rating higher than the peak current it will experience during circuit operation (1A). Less than 300 mΩ ESR is suggested for high efficiency. Open core inductors cause flux linkage with circuit components and interfere with the normal operation of the circuit. This should be avoided. For high efficiency, choose an inductor with a high frequency core material such as ferrite to reduce the core losses. To minimize radiated noise, use a toroid, pot core or shielded core inductor. The inductor should be connected to the OUT pin as close to the IC as possible. Examples of suitable inductors are TDK types LLF4017T-100MR90C and VLF4012AT-100MR79 and Coilcraft type DO3314T-103 (unshielded).

List of Recommended External Components

Symbol	Symbol Explanation	Value	Unit	Type
C_{VDD1}	V_{DD1} bypass capacitor	1	µF	Ceramic, X7R
C_{VDD2}	V_{DD2} bypass capacitor	1	µF	Ceramic, X7R
C_{OUT}	Output capacitor from FB to GND	10	µF	Ceramic, X7R/Y5V
C_{IN}	Input capacitor from Battery Voltage to GND	10	µF	Ceramic, X7R/Y5V
C_{VDDIO}	V_{DDIO} bypass capacitor	1	µF	Ceramic, X7R
C_{VDDA}	Internal LDO output capacitor, between V_{DDA} and GND	1	µF	Ceramic, X7R
RT	Oscillator Frequency Bias Resistor	82	kΩ	1% (1)
RDO	DO output pull-up resistor	100	kΩ	
C_{VREF}	Reference Voltage Capacitor, between V_{REF} and GND	100	nF	Ceramic, X7R
L_{BOOST}	Boost converter inductor	10	µH	Shielded, Low ESR, I_{SAT}1A
D_{OUT}	Rectifying Diode, V_F @ Maxload	0.3	V	Schottky Diode
RGB	RGB LED	User Defined See the AN-1293 Application Report (SNVA071) for resistor size calculation.		
R_R, R_G, R_B	Current Limit Resistors			
LEDs	White LEDs			

(1) Resistor RT tolerance change will change the timing accuracy of the RGB block. Also the boost converter switching frequency will be affected.

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Control Registers

All user accessible control registers and register bits are shown in the following table.

ADDR	SETUP	D7	D6	D5	D4	D3	D2	D1	D0
00H	**Control register**	rgb_pwm	rgb_start	cycle[1]	cycle[0]	rsw	gsw	bsw	pfm_mode
01H	**ron**		ron[6]	ron[5]	ron[4]	ron[3]	ron[2]	ron[1]	ron[0]
02H	**roff**		roff[6]	roff[5]	roff[4]	roff[3]	roff[2]	roff[1]	roff[0]
03H	**gon**		gon[6]	gon[5]	gon[4]	gon[3]	gon[2]	gon[1]	gon[0]
04H	**goff**		goff[6]	goff[5]	goff[4]	goff[3]	goff[2]	goff[1]	goff[0]
05H	**bon**		bon[6]	bon[5]	bon[4]	bon[3]	bon[2]	bon[1]	bon[0]
06H	**boff**		boff[6]	boff[5]	boff[4]	boff[3]	boff[2]	boff[1]	boff[0]
07H	**rslope, rduty**	rslope[3]	rslope[2]	rslope[1]	rslope[0]	rduty[3]	rduty[2]	rduty[1]	rduty[0]
08H	**gslope, gduty**	gslope[3]	gslope[2]	gslope[1]	gslope[0]	gduty[3]	gduty[2]	gduty[1]	gduty[0]
09H	**bslope, bduty**	bslope[3]	bslope[2]	bslope[1]	bslope[0]	bduty[3]	bduty[2]	bduty[1]	bduty[0]]
0AH	**wled current 1**	wled1[7]	wled1[6]	wled1[5]	wled1[4]	wled1[3]	wled1[2]	wled1[1]	wled1[0]
0BH	**enables**	overflow	nstby	en_boost	en_flash	en_ambave	en_ambadc	en_4led	en_2led
0CH	**Amb. Light data**	ain[7]	ain[6]	ain[5]	ain[4]	ain[3]	ain[2]	ain[1]	ain[0]
0DH	**boost output**	boost[7]	boost[6]	boost[5]	boost[4]	boost[3]	boost[2]	boost[1]	boost[0]
2AH	**wled current 2**	wled2[7]	wled2[6]	wled2[5]	wled2[4]	wled2[3]	wled2[2]	wled2[1]	wled2[0]
2BH	**ext pwm enable**				en_redpwm	en_greenpwm	en_bluepwm	en_4ledpwm	en_2ledpwm

Default value of each register is 0000 0000 except the following

— boost output default is 0000 0111 = 07h (4.55V).

— enables default is x010 0000 = 20h (boost enabled)

— ext_pwm_enable default is 0001 1100 = 1Ch (RGB_EN control enabled for color outputs)

Register 0Ch all bits (ain[7:0]) and bit D7 in register 0Bh (overflow) are read only. All other bits are read-write.

REVISION HISTORY

Changes from Revision C (May 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	23

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3936SL	ACTIVE	TLGA	NPC	32		TBD	Call TI	Call TI	-40 to 85	LP3936SL	Samples
LP3936SL/NOPB	ACTIVE	TLGA	NPC	32	1000	Green (RoHS & no Sb/Br)	NIAU	Level-3-260C-168 HR	-40 to 85	LP3936SL	Samples
LP3936SLX	ACTIVE	TLGA	NPC	32		TBD	Call TI	Call TI	-40 to 85	LP3936SL	Samples
LP3936SLX/NOPB	ACTIVE	TLGA	NPC	32		TBD	Call TI	Call TI	-40 to 85	LP3936SL	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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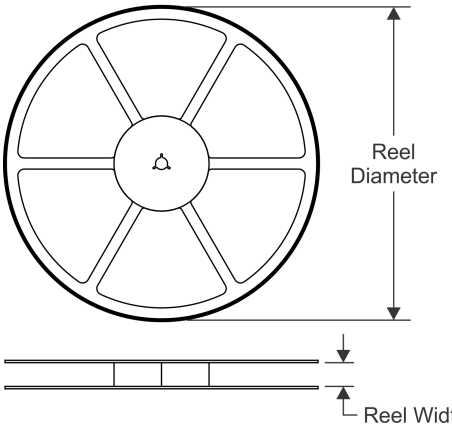
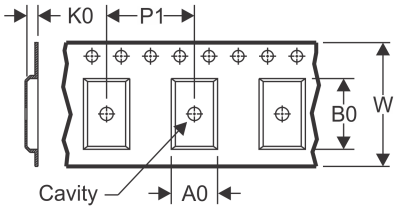
TAPE AND REEL INFORMATION

REEL DIMENSIONS

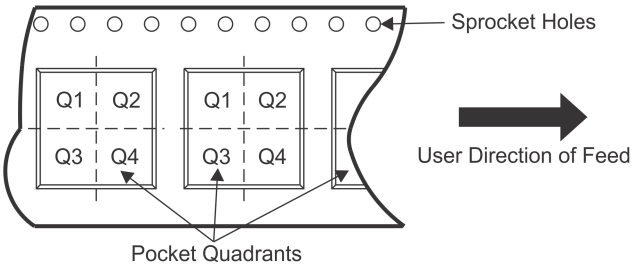


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

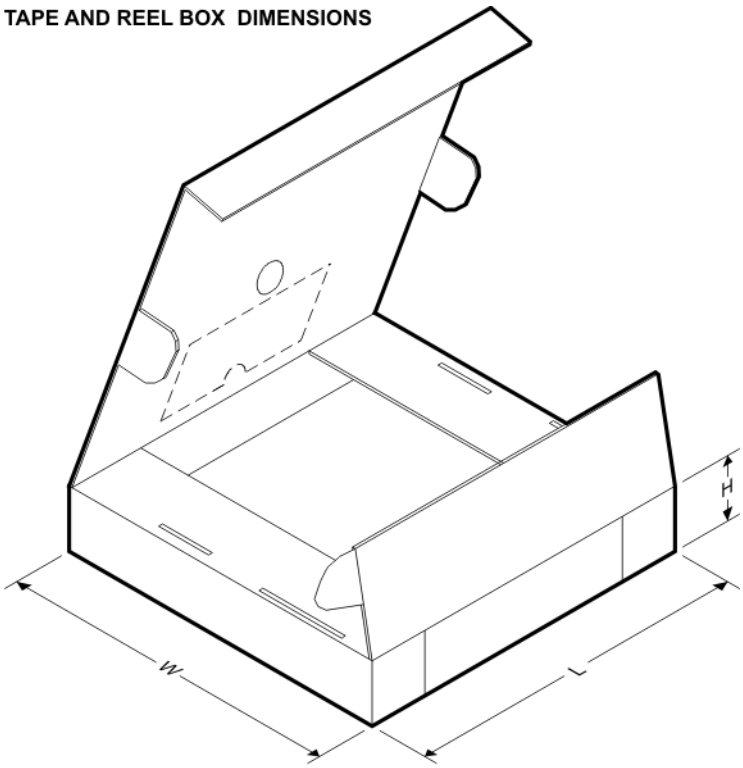
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3936SL	TLGA	NPC	32	1000	178.0	12.4	4.8	5.8	1.3	8.0	12.0	Q1
LP3936SL/NOPB	TLGA	NPC	32	1000	178.0	12.4	4.8	5.8	1.3	8.0	12.0	Q1
LP3936SLX	TLGA	NPC	32	2500	330.0	12.4	4.8	5.8	1.3	8.0	12.0	Q1
LP3936SLX/NOPB	TLGA	NPC	32	2500	330.0	12.4	4.8	5.8	1.3	8.0	12.0	Q1

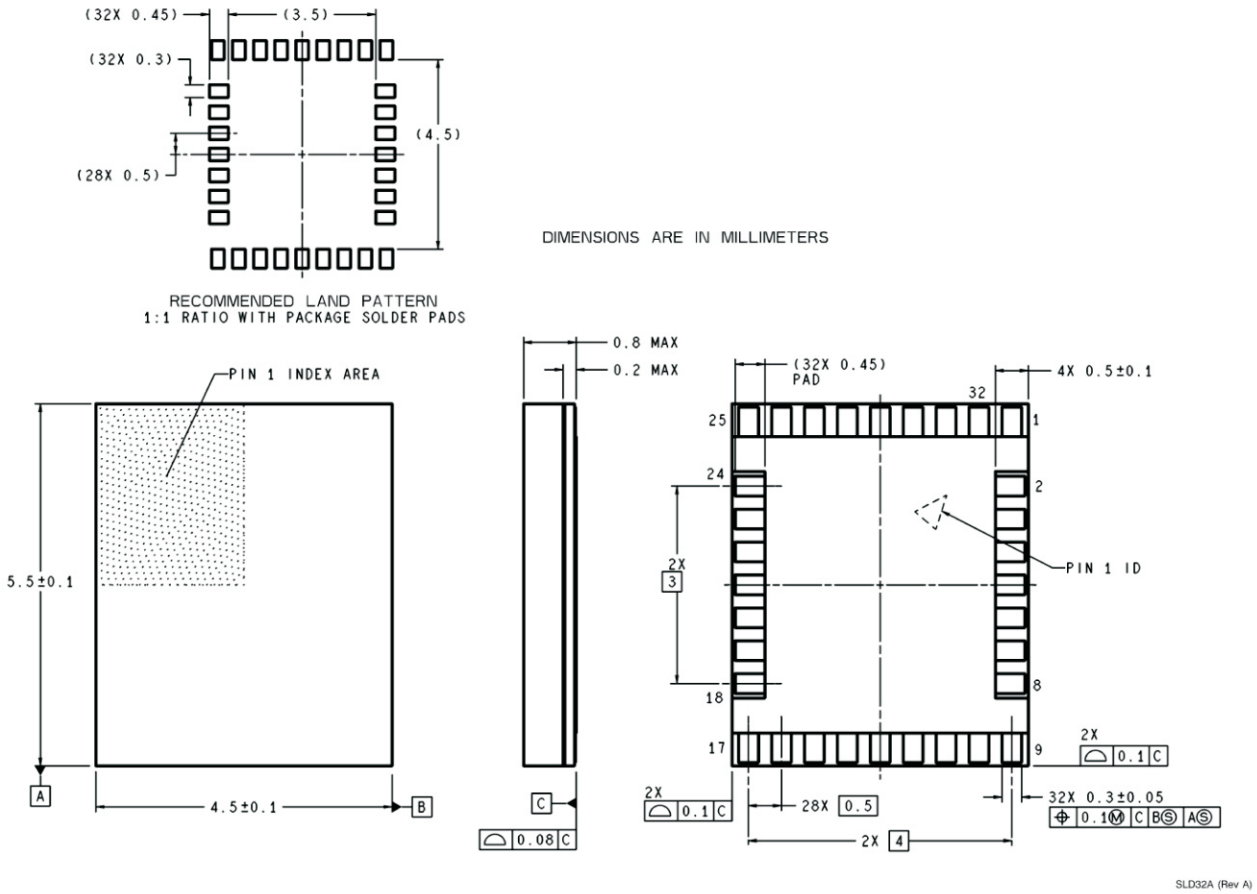
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3936SL	TLGA	NPC	32	1000	213.0	191.0	55.0
LP3936SL/NOPB	TLGA	NPC	32	1000	213.0	191.0	55.0
LP3936SLX	TLGA	NPC	32	2500	367.0	367.0	35.0
LP3936SLX/NOPB	TLGA	NPC	32	2500	367.0	367.0	35.0

NPC0032A


(32X 0.45)
(3.5)
(32X 0.3)
(4.5)
(28X 0.5)
RECOMMENDED LAND PATTERN
1:1 RATIO WITH PACKAGE SOLDER PADS
DIMENSIONS ARE IN MILLIMETERS
PIN 1 INDEX AREA
5.5±0.1
4.5±0.1
A
B
0.8 MAX
0.2 MAX
C
0.08 C
(32X 0.45)
PAD
4X 0.5±0.1
32
25
1
24
2
2X
3
PIN 1 ID
18
8
17
9
2X
0.1 C
2X
0.1 C
28X 0.5
2X 4
32X 0.3±0.05
0.1 M C B S A S
SLD32A (Rev A)

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